DECOUPLING CAPACITOR

ABSTRACT

[0037] A decoupling capacitor with increased resistance to electrostatic discharge (ESD) is provided on an integrated circuit (IC). The capacitor may be single or multi-fingered. In one example, the capacitor includes first and second electrodes separated by a dielectric material, a source positioned proximate to the first electrode, and a floating drain positioned proximate to the first electrode and separated from the source by the first electrode. A parasitic element, modeled as a bipolar junction transistor (BJT), is formed by current interactions between the source, the floating drain, and a doped area. The floating drain provides a constant potential region at the base of the BJT, which minimizes ESD damage to the IC.